KESRX01

Demonstration Receiver A Practical Application

Advance Information

Supersedes September 1996 version, AN207 - 3.0

AN 207 - 4.2 August 1998

This Application Note presents a brief introduction to designing an amplitude shift key (ASK) encoded radio receiver using the KESRX01 super heterodyne receiver operating in the frequency range of 290 to 460MHz. The KESRX01 will work with most industry standard RF frequency encoder and decoder devices. The demonstrator shows the capabilites of KESRX01 and uses a standard digital decoder (Holtec HT–12D, PWM, 8 bit address, 4 bits data) for that purpose.

System Overview

The schematic of the demodulator, Fig. 1, shows the KESRX01 interfaced to a radio frequency PWM decoder chip HT–12D to uniquely encode the receiver.

The complementary PWM encoder chip HT–12E, is used in the transmitter. The RF input to the board is matched to 50Ω to allow direct interfacing to a 50Ω signal generator or 50Ω matched antenna.

The HT–12 chip set uses a pulse width modulated (PWM) 8 bit address to encode/decoder the transmitter or receiver data stream. Synchronisation of the receiver to the transmitter is achieved by setting the HT–12D local oscillator (Fd) at 50 times the received data rate (F t). Upon successful reception of the receiver's unique address, set by the DIL switches, output pin VT is held high indicating that the correctly encoded address has been received and the received data is output on pins D0 to D3. To further increase the redundancy of the system to bit errors the received address is checked 3 times prior to setting the VT pin high and there afterwards. Therefore, output pin VT can be used as a true measure of maximum sensitivity of the receiver for a zero bit error rate.

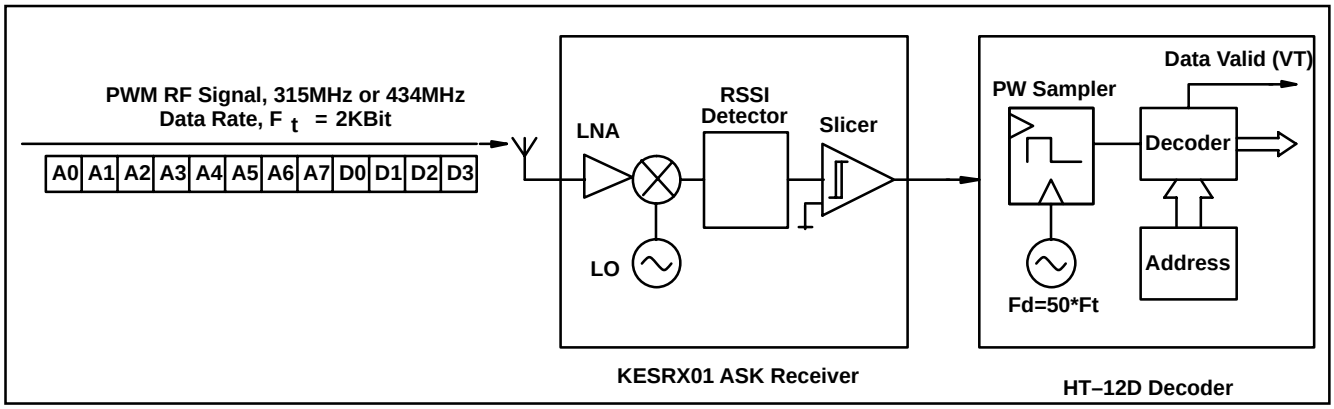

Figure. 1 Block diagram of Demonstrator Receiver

DEMONSTRATION BOARD

Specification

- Typical application for data security for remote control / access control.
- True measurement of receiver performance for a zero bit error rate.
- –103dBm, average power, sensitivity in a 50Ω system for a zero bit error rate using the average configuration.
- Compliance to ETSI 300-220 regulations for a 50Ω system can be achieved.
- Receiver is uniquely 8 bit addressed.
- Capable of receiving an encoded PWM 4 bit data word.

Demonstrator Circuit Configuration

The illustration over page (Fig. 2 and 3) is a block diagram representation for the KESRX01 receiver interfaced to the Holtec HT–12D decoder circuit. Using a 50Ω signal generator operating at 315.022 or 433.90MHz, depending upon component selection, the sensitivity of the system for a zero bit error rate is **typically better than –103dBm**, average power, using the average detector configuration. The complete circuit layout and component parts are shown in Fig. 4. As shown in Fig.2 the data slicer cct. can be implemented in two configurations either ''Peak '' or ''Average'' output to control the operation of the comparator data slicing. The "Peak'' detect output has been designed to squelch the data output when no signal is present so limitingthe maximum sensitivity of the receiver. To maximise the receiver performance the "Average'' output should be used to control the operation of the comparator reference level (DSN) as it has the additional advantage of being able to accommodate variations in extraneous background noise so improving the sensitivity of the device compared to the peak detector mode

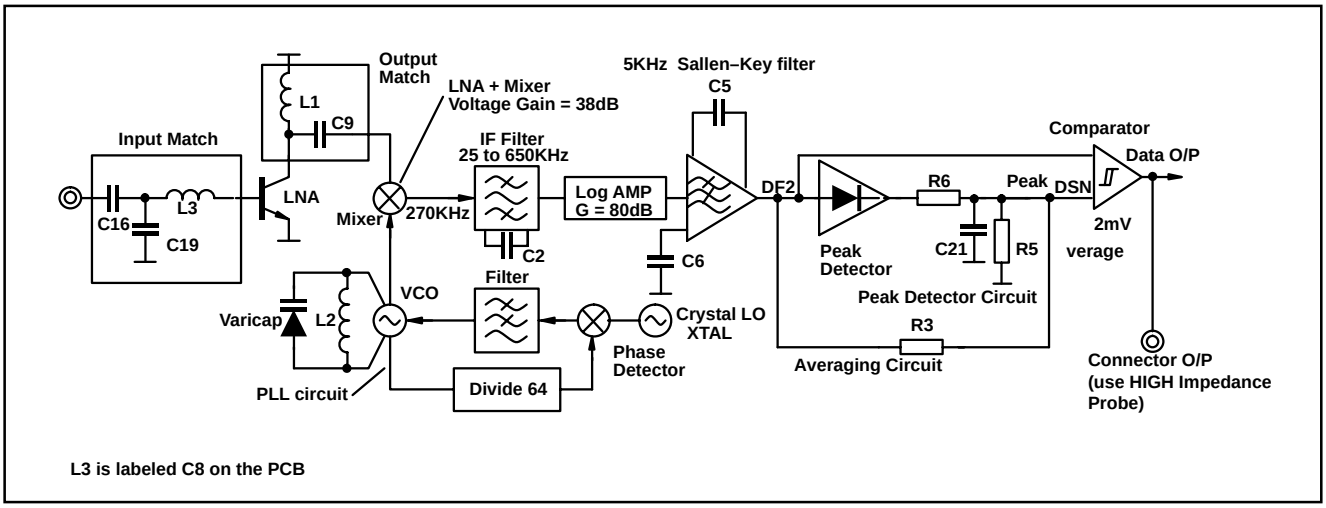

Figure. 2 KESRX01 Receiver block diagram

Connect R6, R5 and C21 for peak detector circuit. Connect R3 and C21 for averaging circuit.

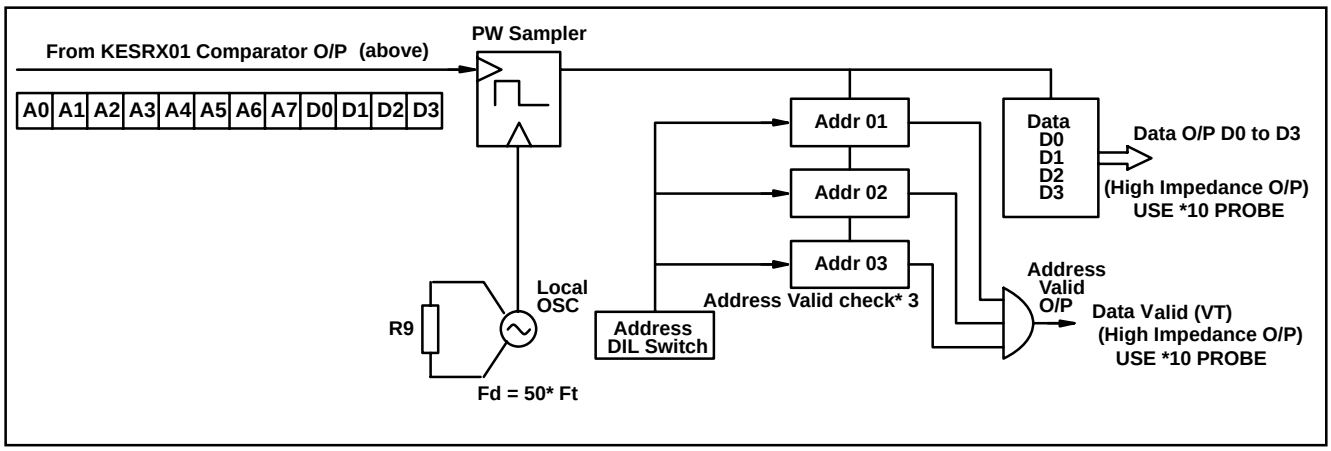

Figure. 3 Holtec HT - 12D block diagram configuration

DEMONSTRATOR PERFORMANCE CHARACTERISTICS

The maximum sensitivity of the receiver for a zero bit error rate and spurious radiations of the receiver have been characterised in a 50Ω system operating at 315.022 and 433.90MHz, using both data slicer configurations. Please note that the maximum sensitivity of the receiver was deemed to be where the LED output connected to output pin VT did not blip ON and OFF indicating that the system performance had not deteriorated from a zero bit error rate condition. To achieve this the signal generator was ASK modulated using a HT12E encoder operating with F t = 2KHz to enable direct communication with the demonstrator.

The results for the above measurements are as follows for the ‘‘Average” and ‘‘Peak” output configurations. Adjacent channel selectivity is the reduction in sesitivity to an interfering signal at 10MHz offset from the wanted signal

		Spurious Conductive Radiations 25MHz to 4GHz		Adjacent Channel selectivity @ 10MHz Spacing	
Mode of operation	Zero Bit Error	Measured value	ETSI Limit	Continuous Tone interferer	Modulated Tone Interfere
Peak	-100dBm @ 315.022MHz	1.9nW	2µW	+10MHz=64.4dB rej	+10MHz=60.9dB rej
Average	-110Bm @ 315.022MHz	1.9nW	2µW	-10MHz=59.9dB rej	-10MHz=55.5dB rej
Peak	-100dBm @ 433.92MHz	1.9nW	2µW	+10MHZ=62.0dB rej	+10MHz=58.9dB rej
Average	-106dBm @ 433.92MHz	1.9nW	2µW	-10MHz=58.9dB rej	-10MHz=54.6dB rej

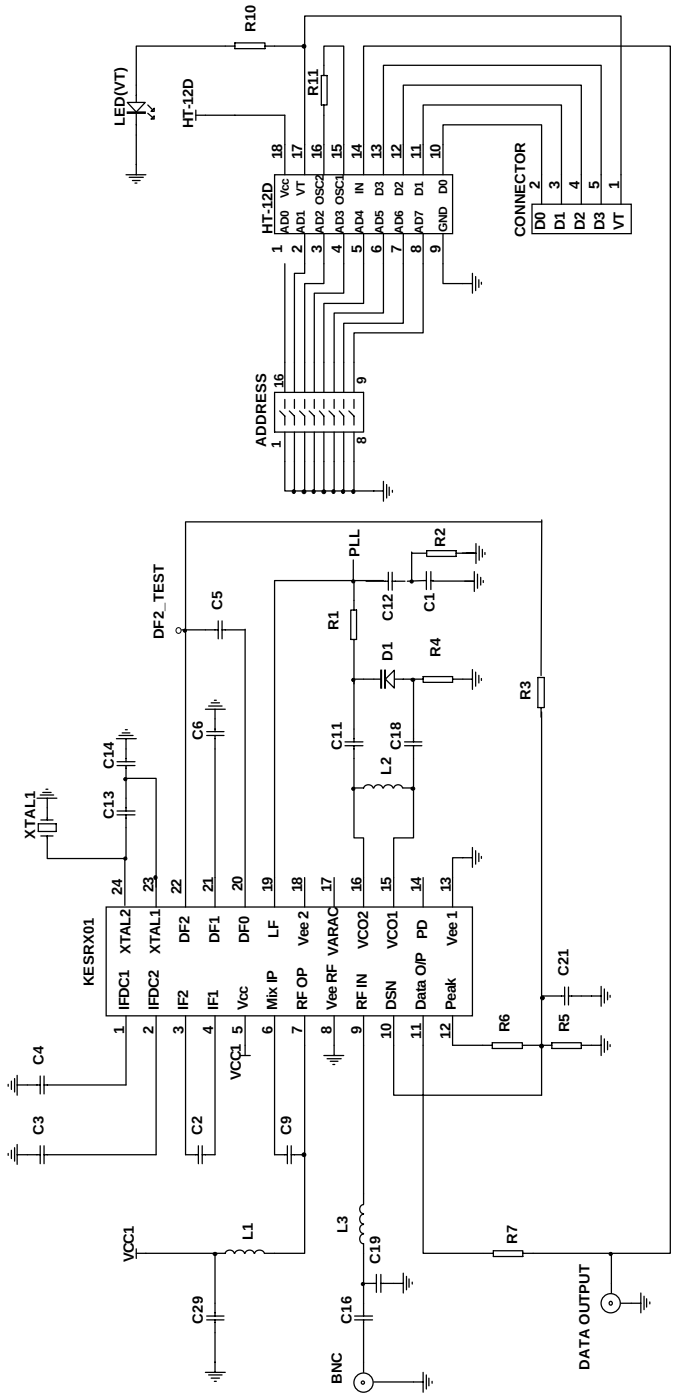

Figure. 4 Demonstration circuit

KESRX01 demonstrator component list for 315MHz and 434MHz application

		Application Circuit	
Circuit Reference	Component Identity	434MHz	315MHz
Supply decoding	C1	150pF	150pF
IF high pass filter	C2	220pF	220pF
Log strip feed back	C3, C4	100nF	100nF
Data filter	C5	220pF	220pF
Data filter	C6	150pF	150pF
LNA/Mixer I/P	C9	56pF	56pF
VCO tank	C11, 18	33pF	33pF
PLL filter	C12	1.5nF	1.5nF
XTAL	C13, C14	18pF	18pF
LNA match	C16	5pF	6pF
LNA match	C19	2pF	2pF
Peak detector	C21	1µF	1µF
Supply decoupling	C29	100pF	100pF
Varactor bias	R1, 4	4.7K	4.7K
Varactor bias	R2	18K	18K
Average circuit	R3	10K	10K
Peak detector	R5	1M	1M
Squelch setting	R6	12 to 27K	12 to 27K
Data O/P	R7	100K	100K
Decoder oscillator	R11	68K	68K
LED brightness	R10	LINK	LINK
LNA output match	L1	47nH	68nH
VCO tank	L2	18nH (27)	39nH (56)
LNA match	L3	68nH	150nH
Decoder	HT12-D	Holtec 8Bit Addr. decoder	Holtec 8Bit Addr. decoder
Varactor	D1	SMV1104-35 or (BBY53-03W)	SMV1104-35 or (BBY53-03W)
Crystal	XTAL1	6.775MHz	4.918MHz

Note: Reducing the value of C3 and C4 to 10nF will improve the response time of the RSSI from power-up (application of Vcc)

Notes:

To select a different data rate the following component values will require adjustment.

- Data filter C5, C6 (for a 10KBit data rate C5=100pF, C6=82pF).
- For optimisation of slice data level R6, R5, C21 and R3 should be adjusted to optimise the sensitivity of the receiver.
- HT-12D Data receive LO frequency (Fd) R9.
- Adjust R6 for maximum sensitivity in squelch mode, “Peak’’ mode. Setting R6 to 27K will guarantee squelch but at the expense of maximum sensitivity, when compared to the “Average’’ mode configuration. The value of R6 is dependent on background noise level and the value chosen for R5 and C21 to squelch the receiver.
- XTAL a <200ppm crystal, parallel resonant at the given frequency with 12pF load capacitor.
- The value of L2 above is for Alpha Industries varactor SMV 1104-35. To use Siemens BBY53-03W, L2 should be :- changed to

Freq	315MHz	434MHz
Varactor	BBY53-03W	BBY53-03W
L2	56nH	27nH

C11 and C18 can be used to fine tune the VCO for a centre tuning control voltage of 2.5V.

- C21 maximum value when operating in the peak detector mode should be less than 220nF. Increasing the value of C21 above 220nF may result in spurious noise spikes appearing at the output of DF2. These spurious noise spikes are caused by supply rail generated noise due to interaction between the peak detector output and the sensitive RF sections of KESRX01 limiting the sensitivity of the receiver
- Connect R5, R6 and C21 for peak detector mode.
- Connect R3 and C21 for averaging mode.
- The component list for AN207 is based on Application Note AN4811
- Gerber files for Application Note AN4811 are freely available from Mitel Semiconductor WWW.
- Additional supply rail decoupling may be required.

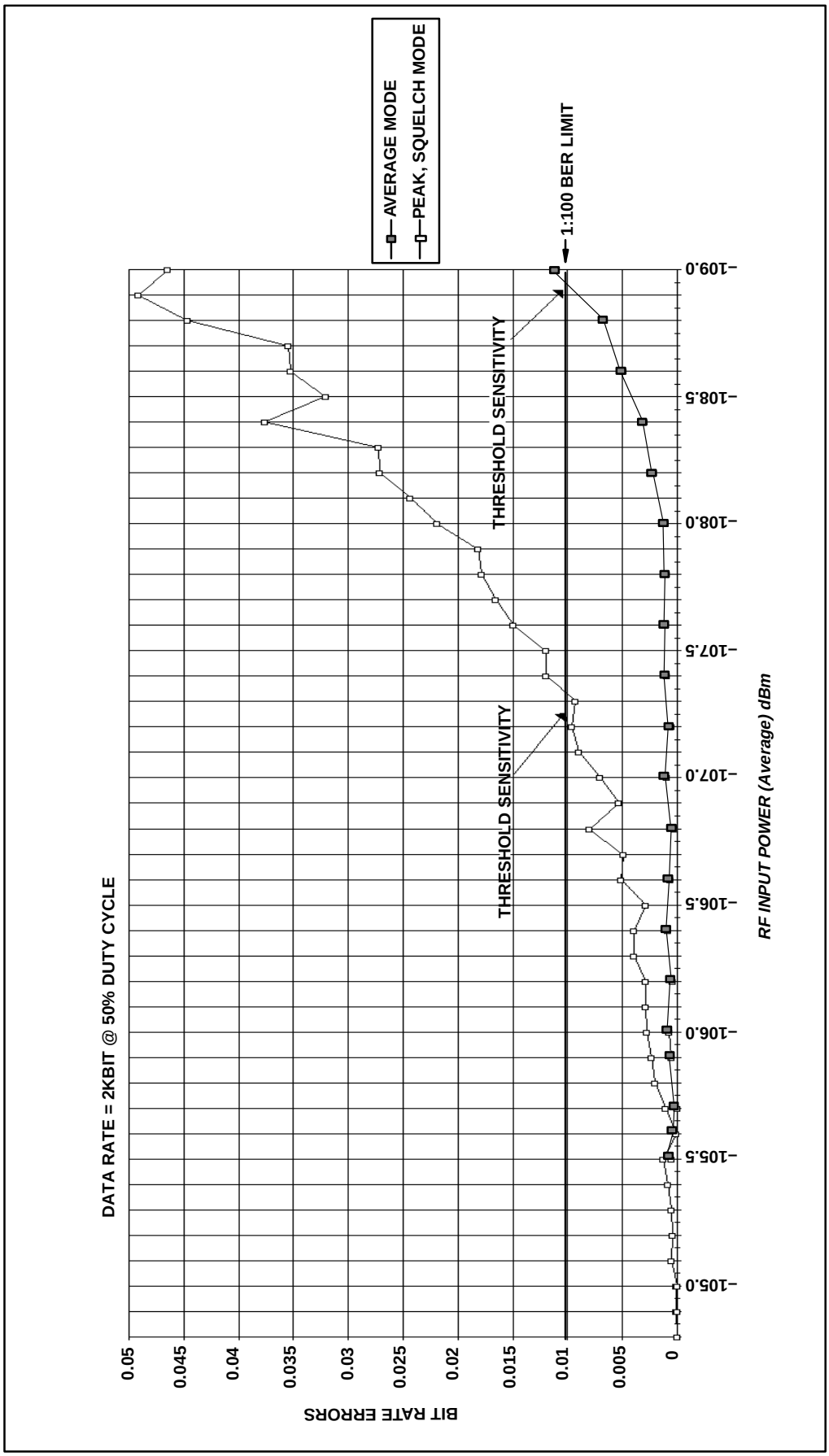

Figure. 5. 434MHz Bit error rate performance

Note. Peak threshold 1/100 BER limit achieved with R6 adjusted for maximum sensitivity.

MITEL

SEMICONDUCTOR

Internet: http://www.mitelsemi.com

CUSTOMER SERVICE CENTRES

- **FRANCE & BENELUX** Les Ulis Cedex
  Tel: (1) 69 18 90 00 Fax: (1) 64 46 06 07
- **GERMANY** Munich Tel: (089) 419508-20 Fax: (089) 419508-55
- **ITALY** Milan Tel: (02) 6607151 Fax: (02) 66040993
- **JAPAN** Tokyo Tel: (03) 5276-5501 Fax: (03) 5276-5510
- **KOREA** Seoul Tel: (2) 5668141 Fax: (2) 5697933
- **NORTH AMERICA** Scotts Valley, USA
  Tel: (408) 438 2900 Fax: (408) 438 5576/6231
- **SOUTH EAST ASIA** Singapore
  Tel:(65) 333 6193 Fax: (65) 333 6192
- **SWEDEN** Stockholm Tel: 46 8 702 97 70 Fax: 46 8 640 47 36
- **TAIWAN, ROC** Taipei Tel: 886 2 25461260 Fax: 886 2 27190260
- **UK, EIRE, DENMARK, FINLAND & NORWAY**
  Swindon Tel: (01793) 726666 Fax : (01793) 518582

These are supported by Agents and Distibutors in major countries worldwide.